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DILWORTH & BARRESE, LLP
333 EARLE OVINGTON BLVD.
SUITE 702
UNIONDALE, NY 11553

EXAMINER	
COLIN, CARL G	
ART UNIT	**PAPER NUMBER**
2136	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	**Application No.** 09/611,518	**Applicant(s)** KIM ET AL.	
	Examiner Carl Colin	**Art Unit** 2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 13 December 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,21,31-47 and 54-70 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,21,31-47 and 54-70 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 20070302.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In response to communications filed on 12/13/2006, claim 54 has been amended. The following claims 1, 21, and 31-47, and 54-70 are presented for examination.

1.1 In response to communications filed on 12/13/2006, the 112[th] rejections of claims 54, 58, 59, 64, 65, 70 have been withdrawn. Applicant has not overcome the double patenting rejection. Therefore, Examiner maintains the rejection.

1.2 Applicant's arguments, pages 10-17, filed on 12/132006, with respect to the rejection of claims 1, 21, and 31-47, and 54-70 have been fully considered, but they are not persuasive. In response to applicant's arguments that adding "the second m-sequence" and "L-times shifted first m-sequence" does in fact result in an Lth secondary scrambling code, and is recited in the claims, applicant is reminded that during patent examination, claims must be given their broadest and reasonable interpretation consistent with the specification. In this instance, the method of claim 1 recites several steps comprising: a step of generating a first m-sequence…; a step of generating a second m-sequence…; a step of masking the first shift register values…; a step of adding the first m-sequence with second m-sequence to generate a primary scrambling code; and a step of adding the third m-sequence and the second m-sequence to generate a secondary scrambling code; and further recites wherein the masking step [masking the first shift register with a first set of mask values to generate a third m-sequence] shifts the first m-sequence cyclically by L chips

to generate an Lth secondary scrambling code associated with the primary scrambling code. Examiner asserts that the claim in its broadest and reasonable interpretation does not recite the adding "the second m-sequence" and the shifting the first m-sequence cyclically by L chips generate an Lth secondary scrambling code associated with the primary scrambling code because as understood by the Examiner and as recited in the claim, the masking step alone generates an Lth secondary scrambling code associated with the primary scrambling code. Regarding the prior art rejection of claims 1 and 21, applicant argues that Burns makes no reference to cyclically shifting an m-sequence to generate a secondary scrambling code (page 13 last paragraph of applicant's response) and adds on page 14, third paragraph that Burns' masking process is not directed to a m-sequence. Examiner respectfully disagrees. As pointed out by Examiner during the conversation held with Applicant's Representative on 2/28/07, column 8, lines 45-61 clearly explains the masking process of Burns. The shift register values are multiplied and combined with adder to produce new values (sequence) in a cyclic process, each value of the sequence is then applied to a register value to produce new state value for each state a new state may be provided which corresponds to a value of the PN sequence shifted by an offset delay and then combining with the mask value to produce offset sequence (scrambling code). (See also column 3, line 40 through column 4, line 5 and figs. 1-4). Burns discloses masking by cyclically shifting and discloses adding masking sequences to generate code sequence or scrambling code, and even discloses adding mask sequence with another sequence. It is noted that the claimed invention is not directed to code assignments contrarily to the statement made by applicant on page 14, paragraph 4 of applicant's response; it is merely reciting steps for generating codes, and was previously discussed on page 4 of the Final rejection

dated 12/28/05. With respect to claim 54, applicant argues that the prior art does not disclose generating a ((K-1)*M +K)th gold code as a Kth primary scrambling code where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code. As interpreted by Examiner, the claim recites generating an unknown number of gold code as primary scrambling with an unknown number of secondary scrambling code per one primary scrambling code. Dahlman et al at least discloses generating gold codes as primary scrambling code Cj and numbers of secondary scrambling codes to be used (Cj1, Cj2) are derived from each primary scrambling code (see column 4, lines 34-57 and column 6, lines 18-59) that meets the claimed limitation. With respect to claims 54 and 65 adding shifted sequence with another sequence is disclosed by Burns as explained above with reference to column 8, lines 45-61. With respect to claims 59 and 65, the prior art discloses generator to generate a first m-sequence and a second m-sequence (see for example Dahlman figure 4). Applicant has not overcome the rejection. Therefore, claims 1, 21, and 31-47, and 54-70 are still rejected in view of the cited prior art.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 21, 31-47, 54-70 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-32 of copending Application No. 11/003,558. Although the conflicting claims are not identical, they are not patentably distinct from each other because the difference between the claims is that the present application generates primary scrambling code by adding the first and the second m-sequences without masking the first m-sequence with respect to claims 1 and 21. Masking provides the advantage of increasing the number of available codes, but may be disadvantageous in processing time and speed as it requires a more complex architecture and processing. It would have been obvious to one of ordinary skill in the art to generate primary scrambling code without masking the first m-sequence in order to save in processing time and also to use a less complex architecture. Application No. 11/003,558 uses masking of the first m-sequence before adding.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 21, 31-47 and 54-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,339,646 to **Dahlman et al.** in view of Foreign Patent Publication WO 99/12284 to **Dahlman** and in view of US Patent 6,141,374 to **Burns**.

As per claim 1, **Dahlman et al.** substantially teaches a method for generating a primary scrambling code (see figure 4) the method comprising: generating a first a first m-sequence from a first m-sequence generator, including first shift registers having first shift register values a_i wherein (i = 0 to c- 1 and where c is the total number of the first registers) (see column 4, line 59 through column 5, line 16); generating a second m-sequence from a second m-sequence generator, including second shift registers having second shift register values bj wherein j = 0 to c-1 where c = the total number of second registers) (see figure 4); adding the first m-sequence

and the second m-sequence to generate a primary scrambling code (see figure 4); **Dahlman et al** also suggests using plurality of adders for combining channelization codes and scrambling codes to produce other secondary scrambling codes or use a modified value or different code phase and not limited to any variations and rearrangements (see column 5, lines 18-35 column 4, lines 40-57). **Dahlman et al** discloses masking step adapted to shift m-sequence by L chips to generate a number of secondary scrambling associated with a primary scrambling code (column 4, line 57 through column 5, line 27 and column 4, lines 2-57). **Dahlman et al** teaches details of assigning codes in a related Foreign application by Dahlman as mentioned in column 1, lines 45-49. **Dahlman** in a Foreign Patent Publication WO 99/12284 discloses assigning spreading codes to base stations (see WO 99/12284 figure 5, 7, and 8 with description). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method described in US Patent 6,339,646 to **Dahlman et al** to generate the scrambling codes and combining it with the teaching in the Foreign Publication WO 99/12284 to assign the codes to the base stations. The motivation or suggestion to do so is given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes and refers to the foreign publication for generating and assigning multiple code sets (column 1, lines 36-48). **Dahlman et al** does not explicitly disclose masking by shifting the sequences cyclically by multiplying with a mask value. **Burns** in an analogous art teaches a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence and further discloses a masking section shifts m-sequence cyclically by L chips to generate a number of secondary scrambling associated with a primary scrambling code and further discloses adding the masking sequence with another sequence (see column 3,

line 40 through column 4, line 5) and also discloses the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the masking concept of multiplying as disclosed in **Burns** before adding the sequence in **Dahlman** to generate secondary scrambling codes associated with the primary scrambling codes. The motivation to do so is given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes (column 1, lines 36-48) and **Burns** suggests shifts are multiplied to produce new values then the combined masks are then added to produce new state values (column 8, lines 45-61).

As per claim 21, **Dahlman et al.** substantially teaches a scrambling code generator (see figure 4) comprising: a first m-sequence generator to generate a first a first m-sequence, by using a plurality of registers with values a_i wherein (i = 0 to c- 1 and where c is the total number of the first registers) (see column 4, line 59 through column 5, line 16); a second m-sequence generator for generating a second m-sequence, by using a plurality of second registers with second-shift register values j = 0 to c-1 where c = the total number of second registers) (see figure 4); a first adder to add the first m-sequence and the second m-sequence to generate a primary scrambling code (see figure 4); **Dahlman et al** also suggests using plurality of adders for combining channelization codes and scrambling codes to produce other secondary scrambling codes or use a modified value or different code phase and not limited to any variations and rearrangements (see column 5, lines 18-35 column 4, lines 40-57). **Dahlman et al** discloses masking step adapted to shift m-sequence by L chips to generate a number of secondary scrambling associated with a

primary scrambling code (column 4, line 57 through column 5, line 27 and column 4, lines 2-57). **Dahlman et al** teaches details of assigning codes in a related Foreign application by Dahlman as mentioned in column 1, lines 45-49. **Dahlman** in a Foreign Patent Publication WO 99/12284 discloses assigning spreading codes to base stations (see WO 99/12284 figure 5, 7, and 8 with description). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method described in US Patent 6,339,646 to **Dahlman et al** to generate the scrambling codes and combining it with the teaching in the Foreign Publication WO 99/12284 to assign the codes to the base stations. The motivation or suggestion to do so is given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes and refers to the foreign publication for generating and assigning multiple code sets (column 1, lines 36-48). **Dahlman et al** does not explicitly disclose masking by shifting the sequences cyclically by multiplying with a mask value. **Burns** in an analogous art teaches a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence and further discloses a masking section shifts m-sequence cyclically by L chips to generate a number of secondary scrambling associated with a primary scrambling code and further discloses adding the masking sequence with another sequence (see column 3, line 40 through column 4, line 5) and also discloses the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the masking concept of multiplying as disclosed in **Burns** before adding the sequence in **Dahlman** to generate secondary scrambling codes associated with the primary scrambling codes. The motivation to do so is

given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes (column 1, lines 36-48) and **Burns** suggests shifts are multiplied to produce new values then the combined masks are then added to produce new state values (column 8, lines 45-61).

As per claims 34, and 41, the combined references disclose the limitation of wherein the masking step is expressed by summing ($K_i \times a_i$) (see **Burns,** column 8, lines 29-61 and figure 4). Therefore, these claims are rejected on the same rationale as the rejection of claims 1 and 21.

As per claims 31-32 and 38-39, the combined references disclose N number of primary scrambling codes and a total number of secondary scrambling codes for each primary code and further discloses a plurality of secondary scrambling codes associated with each primary scrambling code that meets the recitation of wherein the primary scrambling code is one of a plurality of primary scrambling codes and a Kth primary scrambling code is a ((K-1)*M +K)th gold code where M is a total of secondary scrambling codes per primary scrambling code and K is between 1 and 512 and wherein the secondary scrambling codes associated with a Kth primary scrambling code are from ((K-1)*M +K+1)th to ((K-1)*M +K+1)th gold codes where M is a total of secondary scrambling codes per primary scrambling code and K is between 1 and 512 (see **Dahlman et al,** column 6, lines 18-59 and see WO 99/12284 figure 5, 7, and 8 with description).

As per claims 33 and 36, the combined references disclose generating a plurality of secondary codes for one set of primary scrambling code (see **Dahlman et al,** column 5, lines 3-18 and lines 43-47).

Claims 35 and 40 recite similar limitations to claims 1 and 21 performing the same method to generate additional code by using an additional masking value for generating an additional sequence. The combined references disclose generating Nth secondary codes. Therefore, claims 35 and 40 are still obvious since this modification requires routine skill in the art, these claims are rejected on the same rationale as the rejection of claims 1 and 21.

As per claims 37 and 47, the combined references disclose the limitation of further comprising the step of delaying at least one of the primary scrambling code and secondary scrambling code to produce a Q-channel component wherein the primary scrambling code and secondary scrambling code are I-channel components (see **Burns,** column 6, lines 1-14 and column 3, lines 53-57). Therefore, these claims are rejected on the same rationale as the rejection of claims 1 and 21.

As per claim 42, the combined references disclose the limitation of wherein the first m-sequence generator is adapted to cyclically shifting the first shift register values and the second m-sequence generator is cyclically shifts the second shift register values (see **Dahlman et al,** figure 4 and **Burns** column 8, lines 45-61 and figure 4).

As per claims 43 and 45, the combined references disclose the limitation of wherein the first m-sequence generator is adds predetermined bits of the first shift register values of the first shift registers based on the first generator polynomial of the first m-sequence, right shifting the first shift.register values a_i of the first shift registers and replacing the first register value a_{c-1} with the result of the addition of the predetermined register values (see **Dahlman et al**, figure 4 and **Burns** column 8, lines 45-61 and see figure 4).

As per claims 44 and 46 **Dahlman et al.** discloses the limitation of wherein the first m-sequence generator is adds the first shift register value a_0 with a_7 to form a next a_{c-1} and b_0 is added with b_5, b_7, and b_{10} to form a next b_{c-1} (see figure 4).

As per claim 54, **Dahlman et al.** substantially teaches a method for generating scrambling codes in mobile communication system having a scrambling code generator, the method comprising steps of: generating number of primary scrambling codes and a total number of secondary scrambling codes for each primary code and further discloses a plurality of secondary scrambling codes associated with each primary scrambling code (see column 4, lines 34-57 and column 6, lines 18-59); as interpreted by Examiner, the claim recites generating an unknown number of gold code as primary scrambling with an unknown number of secondary scrambling code per one primary scrambling code. Dahlman et al at least discloses generating gold codes as primary scrambling code Cj and numbers of secondary scrambling codes to be used (Cj1, Cj2) are derived from each primary scrambling code (see column 4, lines 34-57 and column 6, lines 18-59), which meets the recitation of generating a ((K-1)*M +K)th gold code as

a Kth primary scrambling code where K is natural number and M is a total number of secondary scrambling codes per primary scrambling code and generating (K-1)*M +K+1)th to ((K-1)*M +K+1)th gold codes as secondary scrambling codes associated with the Kth primary scrambling code, wherein the Lth Gold code is generated by adding an L-1 times shifted first m-sequence and a second m-sequence. **Dahlman et al** discloses masking step adapted to shift m-sequence by L chips to generate a number of secondary scrambling associated with a primary scrambling code (column 4, line 57 through column 5, line 27 and column 6, lines 18-59). **Dahlman et al** teaches details of assigning codes in a related Foreign application by Dahlman as mentioned in column 1, lines 45-49. **Dahlman** in a Foreign Patent Publication WO 99/12284 discloses assigning spreading codes to base stations (see WO 99/12284 figure 5, 7, and 8 with description). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method described in US Patent 6,339,646 to **Dahlman et al** to generate the scrambling codes and combining it with the teaching in the Foreign Publication WO 99/12284 to assign the codes to the base stations. The motivation or suggestion to do so is given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes and refers to the foreign publication for generating and assigning multiple code sets (column 1, lines 36-48). **Dahlman et al** does not explicitly disclose masking by shifting the sequences cyclically by multiplying with a mask value. **Burns** in an analogous art teaches a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence and further discloses a masking section shifts m-sequence cyclically by L chips to generate a number of secondary scrambling associated with a primary scrambling code and further discloses adding the masking sequence with another

sequence (see **Burns,** column 3, line 40 through column 4, line 5) and also discloses the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the masking concept of multiplying as disclosed in **Burns** before adding the sequence in **Dahlman** to generate secondary scrambling codes associated with the primary scrambling codes. The motivation to do so is given by **Dahlman et al** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes (see US Patent 6,339,646 to Dahlman et al; column 1, lines 36-48) and **Burns** suggests shifts are multiplied to produce new values then the combined masks are then added to produce new state values (see **Burns,** column 8, lines 45-61).

As per claim 55, the combined references disclose N number of primary scrambling codes and a total number of secondary scrambling codes for each primary code that meets the recitation of wherein K is a primary scrambling code number and K is between 1 and 512 (see **Dahlman et al,** column 6, lines 18-59 and see WO 99/12284 figure 5, 7, and 8 with description). Claim 55 is therefore rejected on the same rationale as the rejection of claim 54.

As per claim 56, the combined references disclose wherein the first m-sequence is generated from a first shift register memory, by using a plurality of registers with values a_i wherein ($i = 0$ to $c-1$ and where c is the total number of the first registers); (see **Dahlman et al,** column 4, line 59 through column 5, line 16). **Burns** discloses a masking section shifts m-sequence cyclically, the masking is expressed by multiplying mask codes by register values (see

Burns, column 8, lines 29-67 and figures 3 and 4). Claim 56 is therefore rejected on the same rationale as the rejection of claim 54.

As per claim 57, the combined references disclose the limitation of wherein the masking step is expressed by summing (K_i x a_i) (see **Burns,** column 8, lines 29-61 and figure 4). Therefore, claim 57 is rejected on the same rationale as the rejection of claim 54.

As per claim 58, the combined references disclose the limitation of wherein the primary scrambling code and secondary scrambling code are I-channel components and delaying at least one of the primary scrambling code and secondary scrambling code to produce a Q-channel component (see **Burns,** column 6, lines 1-14 and column 3, lines 53-57). Therefore, claim 58 is rejected on the same rationale as the rejection of claim 54.

As per claim 59, **Dahlman et al.** substantially teaches an apparatus for generating scrambling code having scrambling code generator (see figure 4) comprising: a first m-sequence generator to generate a first a first m-sequence, (see column 4, line 59 through column 5, line 16); a second m-sequence generator for generating a second m-sequence, (see figure 4); a first adder to add the first m-sequence and the second m-sequence to generate a primary scrambling code (see figure 4); **Dahlman et al** also suggests using plurality of adders for combining channelization codes and scrambling codes to produce other secondary scrambling codes or use a modified value or different code phase and not limited to any variations and rearrangements (see column 5, lines 18-35 column 4, lines 40-57). **Dahlman et al** discloses masking step adapted to

shift m-sequence by L chips to generate gold code as primary scrambling code (see column 4, lines 40-44 and column 6, lines 18-59). **Dahlman et al** teaches details of assigning codes in a related Foreign application by Dahlman as mentioned in column 1, lines 45-49. **Dahlman** in a Foreign Patent Publication WO 99/12284 discloses assigning spreading codes to base stations where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code (see WO 99/12284 figure 5, 7, and 8 with description). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method described in US Patent 6,339,646 to **Dahlman et al** to generate the scrambling codes and combining it with the teaching in the Foreign Publication WO 99/12284 to assign the codes to the base stations. The motivation or suggestion to do so is given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes and refers to the foreign publication for generating and assigning multiple code sets (column 1, lines 36-48). **Dahlman et al** does not explicitly disclose masking by shifting the sequences cyclically by multiplying with a mask value. **Burns** in an analogous art teaches a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence and further discloses a masking section shifts m-sequence cyclically by L chips to generate a number of secondary scrambling associated with a primary scrambling code and further discloses adding the masking sequence with another sequence (see **Burns,** column 3, line 40 through column 4, line 5) and also discloses the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the masking concept of multiplying as disclosed in

Burns before adding the sequence in **Dahlman** to generate secondary scrambling codes associated with the primary scrambling codes. The motivation to do so is given by **Dahlman et al** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes (see US Patent 6,339,646 to Dahlman et al; column 1, lines 36-48) and **Burns** suggests shifts are multiplied to produce new values then the combined masks are then added to produce new state values (see **Burns,** column 8, lines 45-61).

As per claim 60, the combined references disclose the limitation of wherein the secondary scrambling codes of the Kth primary scrambling code are ((K-1)*M +K+1)th to ((K-1)*M +K+1)th gold codes (see **Dahlman et al,** column 6, lines 18-59 and see WO 99/12284 figure 5, 7, and 8 with description). Claim 60 is therefore rejected on the same rationale as the rejection of claim 59.

As per claim 61, the combined references disclose N number of primary scrambling codes and a total number of secondary scrambling codes for each primary code that meets the recitation of wherein K is a primary scrambling code number and K is between 1 and 512 (see **Dahlman et al,** column 6, lines 18-59 and see WO 99/12284 figure 5, 7, and 8 with description). Claim 61 is therefore rejected on the same rationale as the rejection of claim 59.

As per claim 62, the combined references disclose wherein the first m-sequence generator to generate a first a first m-sequence, by using a plurality of registers with values a_i wherein (i = 0 to c- 1 and where c is the total number of the first registers); (see **Dahlman et al,** column 4,

line 59 through column 5, line 16). **Burns** discloses a masking section shifts m-sequence cyclically, the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Claim 62 is therefore rejected on the same rationale as the rejection of claim 59.

As per claim 63, the combined references disclose the limitation of wherein the masking step is expressed by summing ($K_i \times a_i$) (see **Burns,** column 8, lines 29-61 and figure 4). Therefore, claim 63 is rejected on the same rationale as the rejection of claim 59.

As per claim 64, the combined references disclose the limitation of wherein the primary scrambling code and secondary scrambling code are I-channel components and delaying at least one of the primary scrambling code and secondary scrambling code to produce a Q-channel component (see **Burns,** column 6, lines 1-14 and column 3, lines 53-57). Therefore, claim 64 is rejected on the same rationale as the rejection of claim 59.

As per claim 65, **Dahlman et al.** substantially teaches a method for generating scrambling code having scrambling code generator (see figure 4) comprising: generating a first a first m-sequence, (see column 4, line 59 through column 5, line 16); generating a second m-sequence, (see figure 4); a first adder to add the first m-sequence and the second m-sequence to generate a primary scrambling code (see figure 4). As interpreted by Examiner, the claim recites generating an unknown number of gold code as primary scrambling with an unknown number of secondary scrambling code per one primary scrambling code. Dahlman et al at least

discloses generating gold codes as primary scrambling code Cj and numbers of secondary scrambling codes to be used (Cj1, Cj2) are derived from each primary scrambling code (see column 4, lines 34-57 and column 6, lines 18-59) **Dahlman et al** also suggests using plurality of adders for combining channelization codes and scrambling codes to produce other secondary scrambling codes or use a modified value or different code phase and not limited to any variations and rearrangements (see column 5, lines 18-35 column 4, lines 40-57), which meets the recitation of generating a ((K-1)*M +K)th gold code as a Kth primary scrambling code where K is natural number and M is a total number of secondary scrambling codes per primary scrambling code and generating (K-1)*M +K+1)th to ((K-1)*M +K+1)th gold codes as secondary scrambling codes associated with the Kth primary scrambling code. **Dahlman et al** discloses masking step adapted to shift m-sequence by L chips to generate gold code as primary scrambling code (see column 4, lines 40-44 and column 6, lines 18-59). **Dahlman et al** teaches details of assigning codes in a related Foreign application by Dahlman as mentioned in column 1, lines 45-49. **Dahlman** in a Foreign Patent Publication WO 99/12284 discloses assigning spreading codes to base stations where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code (see WO 99/12284 figure 5, 7, and 8 with description). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method described in US Patent 6,339,646 to **Dahlman et al** to generate the scrambling codes and combining it with the teaching in the Foreign Publication WO 99/12284 to assign the codes to the base stations. The motivation or suggestion to do so is given by **Dahlman** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes and refers to the

foreign publication for generating and assigning multiple code sets (column 1, lines 36-48). **Dahlman et al** does not explicitly disclose masking by shifting the sequences cyclically by multiplying with a mask value. **Burns** in an analogous art teaches a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence and further discloses a masking section shifts m-sequence cyclically by L chips to generate a number of secondary scrambling associated with a primary scrambling code and further discloses adding the masking sequence with another sequence (see **Burns,** column 3, line 40 through column 4, line 5) and also discloses the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the masking concept of multiplying as disclosed in **Burns** before adding the sequence in **Dahlman** to generate secondary scrambling codes associated with the primary scrambling codes. The motivation to do so is given by **Dahlman et al** who suggests that additional scrambling codes can be used to increase the number of available codes to avoid a shortage of codes (see US Patent 6,339,646 to Dahlman et al; column 1, lines 36-48) and **Burns** suggests shifts are multiplied to produce new values then the combined masks are then added to produce new state values (see **Burns,** column 8, lines 45-61).

As per claim 66, the combined references disclose the limitation of wherein the secondary scrambling codes of the Kth primary scrambling code are ((K-1)*M +K+1)th to ((K-1)*M +K+1)th gold codes (see **Dahlman et al,** column 6, lines 18-59 and see WO 99/12284

figure 5, 7, and 8 with description). Claim 66 is therefore rejected on the same rationale as the rejection of claim 65.

As per claim 67, the combined references disclose N number of primary scrambling codes and a total number of secondary scrambling codes for each primary code that meets the recitation of wherein K is a primary scrambling code number and K is between 1 and 512 (see **Dahlman et al,** column 6, lines 18-59 and see WO 99/12284 figure 5, 7, and 8 with description). Claim 67 is therefore rejected on the same rationale as the rejection of claim 65.

As per claim 68, the combined references disclose wherein the first m-sequence is generated from a first shift register memory, by using a plurality of registers with values a_i wherein ($i = 0$ to $c-1$ and where c is the total number of the first registers); (see **Dahlman et al,** column 4, line 59 through column 5, line 16). **Burns** discloses a masking section shifts m-sequence cyclically, the masking is expressed by multiplying mask codes by register values (see **Burns,** column 8, lines 29-67 and figures 3 and 4). Claim 68 is therefore rejected on the same rationale as the rejection of claim 65.

As per claim 69, the combined references disclose the limitation of wherein the masking step is expressed by summing ($K_i \times a_i$) (see **Burns,** column 8, lines 29-61 and figure 4). Therefore, claim 69 is rejected on the same rationale as the rejection of claim 65.

As per claim 70, the combined references disclose the limitation of wherein each scrambling code is used as an I-channel component and a Q-channel component corresponding to the I-channel component is generated by delaying the I-channel component for a predetermined time (see **Burns,** column 6, lines 1-14 and column 3, lines 53-57). Therefore, claim 70 is rejected on the same rationale as the rejection of claim 65.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carl Colin whose telephone number is 571-272-3862. The examiner can normally be reached on Monday through Thursday, 8:00-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser G. Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CC

Carl Colin
Patent Examiner
March 2, 2007

NASSER MOAZZAMI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

3/2/07